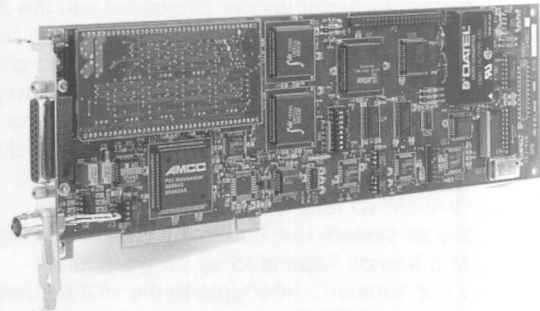


FEATURES

- The ideal array-processor "front end"
- Up to 10MHz A/D sampling rates
- Choice of 12, 14 or 16-bit A/D resolutions
- Wideband inputs with low harmonic distortion
- Quick, 32-bit, PCI block transfers
- 2 to 16-channel simultaneous sampling eliminates phase skew
- On-board A/D FIFO memory holds 8k samples
- 32 megasamples or greater data streaming
- Pre/post-trigger, gap-free, ring buffering
- Great for DSP, FFT's, digital filtering, etc.
- Pentium® compatible; Windows NT software

NEW
Windows® NT
Software



GENERAL DESCRIPTION

The PCI-416 Family consists of several advanced-performance, data acquisition boards based on the 32-bit PCI bus architecture. With an emphasis on continuous, non-stop, high-speed streaming of A/D samples to host memory or disk, the system has been optimized for a wide range of signal-processing and data-recording applications. In very long "baseline" studies or high-speed transient analysis, the PCI-416 can collect more than 64 megabytes of "seamless" digitized data to host memory.

Exploiting a unique "banked" FIFO architecture, the PCI-416 moves two A/D words in each 32-bit PCI transfer. The FIFO memory (8k samples deep) serves to decouple the precise timing of the A/D converter from the block bursts of the PCI bus.

The PCI-416's optional analog front-ends utilize DATEL's low-noise, wide-bandwidth sampling A/D converters. All models exhibit excellent harmonic distortion and perform well in DSP/FFT applications. The PCI-416SET software readily implements a menu-driven, "no-programming", fast data recording system to memory and disk.

Several different "pluggable" analog options offer up to 16 input channels in single-ended or differential configurations, multiple input ranges, sampling rates to 10MHz, 12/14/16-bit A/D resolutions, and various simultaneous sampling configurations (1 A/D per channel) up to 16 channels. The simultaneous feature is intended for parallel sampling applications that cannot tolerate phase skew introduced by the

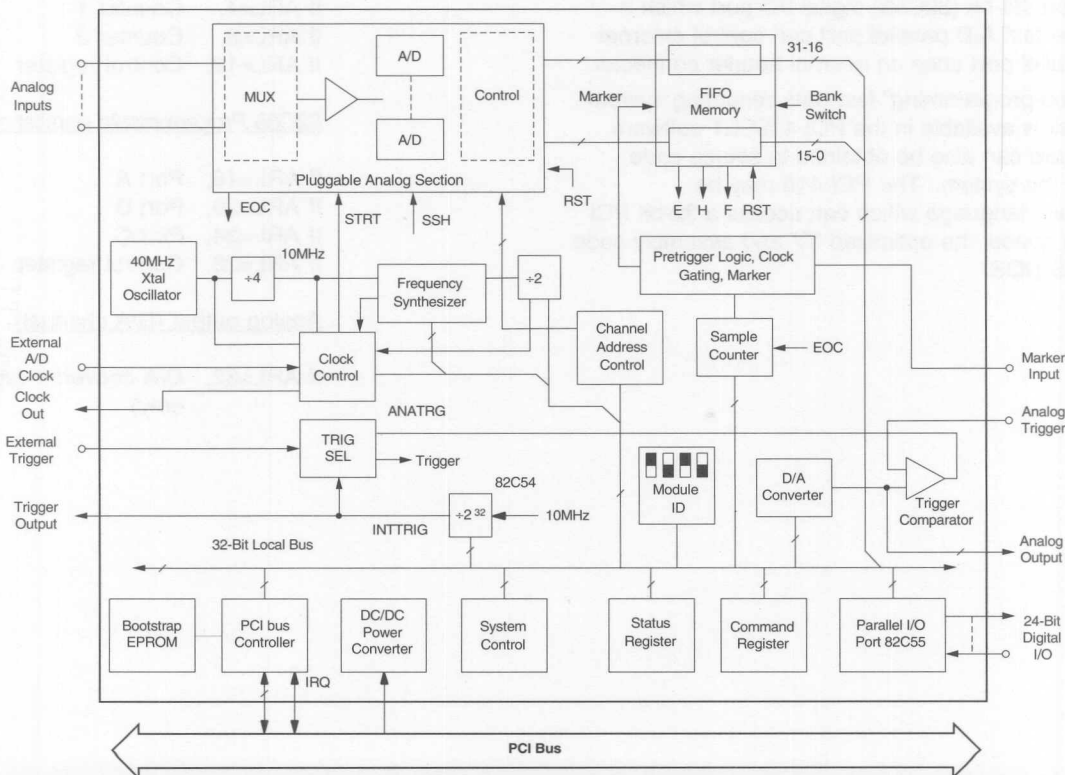


Figure 1. Functional Block Diagram

A/D system. These include sonar or acoustic sensor arrays, cross-channel computation, multiple carrier demodulation, interferometry, multichannel spectrometers, and highly concurrent system testing. High-quality, wide-bandwidth, low-noise A/D's and analog components are used. The design is ideal as an array processor "front end" or for DSP/FFT (Digital Signal Processing/Fast Fourier Transform) usage.

Two on-board software-programmable timebases run the A/D sample clock. A 40MHz frequency synthesizer provides high resolution whereas the 10MHz 16-stage programmable divider offers very low clock jitter. If preferred, external clocks may be accepted for both the A/D start clock and the trigger. And several PCI-416's may be connected in master-slave clocking for many simultaneous channels. A programmable 24-bit sample counter will collect long blocks up to 16 million samples. The trigger system can collect a single fixed length frame, N repeating frames separated by programmable delays, or it can run "forever". Interrupts to the PCI bus are programmable from the FIFO flags, bus master block transfer done, or the sample counter.

System features optimize gapless sampling without data loss. A pretrigger system can collect data continuously to host circular memory (ring buffer) of several megabytes or more. When an external trigger is received, the PCI-416 will count down the number of preloaded post-trigger samples then automatically stop when all samples are collected. The trigger sample may then be found using a negative circular offset into the ring buffer, knowing the post-trigger sample count.

In addition, a digital marker input will tag data samples on the fly as often as needed. This provides later identification of external events without stopping sample collection. A D/A analog output channel is included to set the trip level for external analog triggers. Or the D/A can be used for analog output.

A general-purpose, 24-bit (82C55) digital I/O port which is separate from the fast A/D parallel port can control external circuits. The parallel port uses an internal header connector.

A menu-driven "no-programming" fast data recording system to memory or disk is available in the PCI-416SET software. This "SET" software can also be obtained in source code format to modify the system. The PCI-416 may be programmed in any language which can access a 32-bit PCI bus. For highest speed, the optimized "C" and assembly code is used under MS-DOS.

REGISTER I/O or MEMORY MAPPING

All of the PCI-416's registers require 32-bit instructions. DATEL software provides highly portable examples which can be used with any language. All registers are fully described in the User Manual included with the board.

| Base Address | Register | Function |
|--------------|--------------|--|
| | BADR0 | S5933 PCI controller operation registers |
| | BADR1 | Pass-Thru Address Register Latch (ARL) |
| | BADR2 | Read/Write general registers <ul style="list-style-type: none"> If ARL=0, Command register (write only) If ARL=4, Sample counter (write only) If ARL=8, Channel address register (write) Clear A/D FIFO memory (read) If ARL=12, A/D convert enable (write only) If ARL=16, PLL register (write only) |
| | BADR3 | High-speed read of status register or A/D FIFO data <ul style="list-style-type: none"> If ARL=0, Status register (read only) If ARL=4, A/D FIFO data (read only) |
| | BADR4 | Low-speed devices, 82C54 and 82C55, and analog output <ul style="list-style-type: none"> <u>82C54 Programmable counter-timer</u> (read/write) <ul style="list-style-type: none"> If ARL=0, Counter 0 If ARL=4, Counter 1 If ARL=8, Counter 2 If ARL=12, Control register <u>82C55 Programmable parallel port</u> (read/write) <ul style="list-style-type: none"> If ARL=16, Port A If ARL=20, Port B If ARL=24, Port C If ARL=28, Control register <u>Analog output (D/A channel)</u> <ul style="list-style-type: none"> If ARL=32, D/A converter register (write only) |

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C, dynamic conditions, gain = 1, unless noted)

| ANALOG INPUTS | PCI-416B | PCI-416D | PCI-416E | PCI-416F |
|---|--------------------------|--------------------------------------|--|------------------|
| Number of Channels | 4 | 1 | 16SE/8D | 2 Simultaneous |
| Input Configuration (non-isolated) [Footnote 15] | Single Ended | Differential | SE or Diff. | Single Ended |
| Full Scale Input Ranges (user-selectable) (gain = 1) | 0 to +10V ±10V ±5V | ±5V (0 to +10V, special order) | 0 to +10V ±10V ±5V [Footnote 1] | 0 to +10V ±5V |
| Input Overvoltage (no damage, power on) | ±15V | ±15V | ±15V | ±15V |
| Overvoltage Recovery Time , maximum | 2μs | 2μs | 2μs | 2μs |
| Common Mode Voltage Range , maximum | — | ±1V | ±10V | — |
| Input Impedance | 10MΩ | 2kΩ | 100MΩ | >1MΩ |
| SAMPLE/HOLD | | | | |
| Acquisition Time | 750ns | 50ns | 750ns | 165ns |
| Aperture Delay | 20ns | 10ns | 20ns | 20ns |
| Aperture Delay Uncertainty | ±100ps | ±7ps | ±40ps | ±40ps |
| A/D CONVERTER | | | | |
| Resolution | 14 bits | 12 bits | 12 bits | 12 bits |
| Conversion Period | 1.6μs | 200ns | 500ns | 400ns |
| SYSTEM DC CHARACTERISTICS [Footnote 6] | | | | |
| Integral Non-linearity (LSB of FSR) | ±1.5 | ±2 | ±1 | ±1 |
| Differential Non-linearity (LSB of FSR) | ±1 | ±1 | ±0.75 | ±1 |
| Full Scale Temperature Coefficient (LSB per °C) | ±0.3 | ±0.1 | ±0.1 | ±0.1 |
| Zero or Offset Temperature Coefficient (LSB per °C) | ±0.3 | ±0.3 | ±0.1 | ±0.1 |
| SYSTEM DYNAMIC PERFORMANCE [Footnote 2] | | | | |
| Sample Rate (single channel only) | 500kHz | 5MHz | 2MHz | 2MHz |
| Sample Rate per Channel (simul. or sequential chans.) [Footnote 4] | 82kHz/chan. | — | 31.25kHz/chan. | 2MHz/chan. |
| Total Harmonic Distortion [Footnote 3] | −75dB | −68dB | −72dB | −70dB |

Note: Model PCI-416J in short-cycled addressing is recommended in place of the previously announced PCI-416A.
Model PCI-416E can substitute for the previously announced PCI-416C.

| | | | |
|--|---|-----------------------|---|
| ANALOG INPUTS | | A/D CONVERTER | |
| Programmable Gains | See Footnote 1 | Output Coding | Positive-true, right justified, straight bin. (unipolar) or right-justified 2's comp. (bipolar) with sign extension thru bit 15 |
| Common Mode Rejection (DC - 60Hz) | −80dB (g = 100) (416E) | Warm-Up Period | 20 minutes until rated specifications. [Footnote 6] |
| Addressing Modes (short cycle channel addressing is software-selectable on PCI-416J,L) | 1. Single channel 2. Simultaneous sampling 3. Sequential with autosequenced addressing 4. Random addressing by host software | | |

Please read all footnotes carefully.

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C, dynamic conditions, gain = 1, unless noted)

| ANALOG INPUTS | PCI-416G | PCI-416H | PCI-416J | PCI-416K |
|---|---|--|---|--|
| Number of Channels | 2 Simultaneous | 1 | 8 Simultaneous | 2 Simultaneous |
| Input Configuration (non-isolated) [Footnote 15] | Single Ended | Differential | Single Ended | Limited Differential |
| Full Scale Input Ranges (user-selectable) (gain = 1) | ±5V or 0 to +10V (separate models) | ±5V (other ranges special order) | ±5V, ±10V [Footnote 10] | 0 to +10V, ±5V (separate models) |
| Input Overvoltage (no damage, power on) | ±15V | ±15V | ±15V | ±15V |
| Overvoltage Recovery Time , maximum | 2μs | 1μs | — | — |
| Common Mode Voltage Range , maximum | — | ±1V | — | ±1V |
| Input Impedance | >1MΩ | 2kΩ | 8kΩ (bipolar) | 1kΩ |
| SAMPLE/HOLD | | | | |
| Acquisition Time | 350ns | 35ns | 400ns | 50ns |
| Aperture Delay | 20ns | ±10ns | — | 10ns |
| Aperture Delay Uncertainty | ±70ps | 3ps rms | — | ±7ps |
| A/D CONVERTER | | | | |
| Resolution | 14 bits | 12 bits | 12 bits | 12 bits |
| Conversion Period | 1μsec* | 100ns | 2μs (all chans. in simul. sampling) | 200ns |
| SYSTEM DC CHARACTERISTICS [Footnote 6] | | | | |
| Integral Non-linearity (LSB of FSR) | ±1.5 | ±1.5 | ±1 | ±2 |
| Differential Non-linearity (LSB of FSR) | ±1 | ±1 | ±1 | ±1 |
| Full Scale Temperature Coefficient (LSB per °C) | ±0.3 | ±1 | [Footnote 10] | ±0.1 |
| Zero or Offset Temperature Coefficient (LSB per °C) | ±0.3 | ±1 | [Footnote 10] | ±0.3 |
| SYSTEM DYNAMIC PERFORMANCE [Footnote 2] | | | | |
| Sample Rate (single channel only) | 1MHz* | 10MHz | 400kHz | 5MHz |
| Sample Rate per Channel (simul. or sequential chans.) [Footnote 4] | 1MHz/chan.* | — | 250kHz/chan.** | 5MHz 10MHz (5MHz/ch.) |
| Total Harmonic Distortion [Footnote 3] | −80dB | −65dB | −75dB | −68dB |

*Dual 2MHz 14-bit sampling is available on special order, model PCI-30267.

**A 380kHz/channel option is available on special order, model PCI-30264.

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C, dynamic conditions, gain = 1, unless noted)

| ANALOG INPUTS | PCI-416L | PCI-416M* | PCI-416N* |
|---|--|---|---|
| Number of Channels | 16 Simultaneous | 4 Simultaneous | 2 Simultaneous |
| Input Configuration (non-isolated) [Footnote 15] | Single Ended | Single Ended | Single Ended |
| Full Scale Input Ranges (user-selectable) (gain = 1) | ±5V, ±10V, (user selectable) [Footnote 10] | ±10V | ±2V |
| Input Overvoltage (no damage, power on) | ±15V | ±12V | ±15V |
| Overvoltage Recovery Time, maximum | — | — | — |
| Common Mode Voltage Range, maximum | — | — | — |
| Input Impedance | 8kΩ | 10MΩ | 10MΩ or 50Ω |
| SAMPLE/HOLD | | | |
| Acquisition Time | 400ns | — | 35ns |
| Aperture Delay | — | — | ±10ns |
| Aperture Delay Uncertainty | — | — | 5ps |
| A/D CONVERTER | | | |
| Resolution | 12 bits | 16 bits | 14 bits |
| Conversion Period | 2μs (all chans. in simul. sampling) | 5μs (all chans. in simul. sampling) | 200ns (all chans. in simul. sampling) |
| SYSTEM DC CHARACTERISTICS [Footnote 6] | | | |
| Integral Non-linearity (LSB of FSR) | ±2 | ±4 | ±1 |
| Differential Non-linearity (LSB of FSR) | ±1 | ±3 | ±1 |
| Full Scale Temperature Coefficient (LSB per °C) | [Footnote 10] | ±1 | ±0.5 |
| Zero or Offset Temperature Coefficient (LSB per °C) | [Footnote 10] | ±1 | ±0.5 |
| SYSTEM DYNAMIC PERFORMANCE [Footnote 2] | | | |
| Sample Rate (single channel only) | 400kHz | 200kHz | 8MHz |
| Sample Rate per Channel (simul. or sequential chans.) [Footnote 4] | 190kHz/chan. | 200kHz/chan. | 5MHz/chan. |
| Total Harmonic Distortion [Footnote 3] | -75dB | -83dB | -75dB |

*Preliminary models, specifications subject to change. Call DATEL for latest information.

SPECIFICATIONS, CONTINUED

(Typical @ +25°C, dynamic conditions, unless noted)

| A/D SAMPLE CLOCK | |
|---|---|
| Sample Clock Sources [Footnote 7] | Selectable from among: 1. Frequency synthesizer 2. 10MHz crystal oscillator 3. 20MHz crystal oscillator 4. 16-stage binary divider to either 1 or 2, maximum input: 10MHz |
| Frequency Synthesizer | Output 5-10MHz in 625Hz steps, further divisible by 16-stage binary divider, all software programmable. Up to 40MHz is available in 2500Hz steps. |
| Total Sample Range | 76.3Hz to 10MHz (40MHz available) |
| Oscillator Frequency Accuracy | ±50ppm (+20 to +30°C) |
| Crystal Aging | ±5ppm/year |
| TRIGGER CONTROL | |
| Trigger Sources [Footnote 8] | 1. Analog threshold comparator using internal D/A to set trip level 2. Internal trigger derived from 10MHz timebase, divided by 32-stage divider (82C54). Range: 20ns to 429.5 seconds. 3. External digital trigger |
| Trigger Response | Selectable from among: 1. Starts one frame ("single trigger mode") 2. Collects repeating frames, each started by a trigger ("continuous trigger mode"). 3. Runs the A/D "forever" (sample counter disabled) |
| A/D Samples per Frame | 1 to 16,777,216 samples (24-bit counter) or "forever" |
| Analog Trigger Input Range | ±10V |
| Analog Trigger Response | 2µs [Footnote 5] |
| Analog Trigger Hysteresis | ±40mV |
| Marker Input | Digital input which sets A/D bit 15 to logic "1" for one A/D clock cycle. Used to tag samples to external events if enabled. |
| Pretrigger Mode | The sample down-counter is delayed until an external trigger. Pretrigger samples are stored in a host ring buffer for transient capture, if enabled. |

| ANALOG OUTPUT | |
|------------------------------------|--|
| Number of Channels Function | One channel Selectable from among: 1. General-purpose analog output 2. Threshold comparator for A/D trigger |
| Resolution | 12 bits |
| Output Voltage Range | 0 to +10V, ±5V, ±10V at 5mA max. (user selectable) |
| Linearity | ±0.05% of FSR |
| Settling Time | 5 microseconds (10V step) |
| Input Coding | Straight binary |
| PCI Bus | |
| Data Bus Size | 32 bits |
| Address Bus Size | 32 bits |
| PCI Controller Type | AMCC S5933 bus master or slave mode |
| Data Transfer | 32-bit I/O or memory (selectable) |
| Bus Transfer Mode | Up to 2 ²⁴ longwords, per PCI spec. |
| Interrupt | One interrupt, INTA# only per PCI spec. |
| Interrupt Sources | FIFO half full, sample count reached (ACquire flag), bus master transfer done. |
| MISCELLANEOUS | |
| Board Identification Switch | 4-bit DIP switch is factory preset to identify A/D module type. May be changed if another module is used. |
| Analog Section Modularity | The MUX-S/H-A/D module is socketed for function interchange. |
| Analog Section Adjustments | Offset and gain per channel for SSH on PCI-416F,G. A single offset and gain pot is provided on PCI-416B,D,E. Recommended recalibration interval is 90 days in stable conditions. |
| Operating Temp. Range | 0 to +60°C, thermal shock ±1°C max per minute. |
| Storage Temp. Range | -25 to +85°C |
| Humidity | 10% to 90%, non-condensing |
| Altitude | 0 to 10,000 feet, forced cooling is required |
| Power Required | +5Vdc @ 3.0A max. from PCI bus. Compatible to +3.3V systems but makes no connection. |
| Outline Dimensions | 4.2 x 12.28 x 0.5 inches, compatible to PCI bus |
| A/D MEMORY | |
| Architecture | First-In, First-Out (FIFO) |
| Memory Capacity | 8192 A/D samples |

| CONNECTORS | |
|----------------------------------|---|
| PCI bus | 120-pin (dual 60) PCI edgeboard connector |
| Analog Input | DB-25 25-pin connector mounted on rear plate. Miniature threaded coaxial SMA connectors are available under special order for 4 input channels or less. |
| External Trigger [Footnote 9] | On DB-25 analog connector |
| External A/D Clock In | BNC coaxial on rear plate |
| Digital I/O Port | Internal header connector. External clock, D/A mounted on board interior, suitable for flat cables. |
| DIGITAL I/O PORT | |
| Configuration | 24 lines, programmable as input or output with latches and handshakes |
| Controller Levels | 82C55 TTL logic, 1 TTL load in or out (direct from 82C55) |
| Outport Settling Time | 50ns, after write operation |

FOOTNOTES

- Resistor-programmed gain (user supplied) from x1 to x100 is available on PCI-416E with increased settling delay at higher gains. Requires precision gain resistor.
- Total throughput includes MUX settling time after changing the channel address, S/H acquisition time to rated specifications, A/D conversion, and FIFO transfer. Total throughput is not delayed by host software whenever the FIFO is not full.
- THD test conditions are:
 - Input freq. 500kHz (416F) 200kHz (416B,E,G)
50kHz (416J,L,M) 1MHz (416D,K)
2MHz (416H)
 - Generator/filter THD is -90dB minimum.
 - THD computed by FFT to 5th harmonic.

$$THD = 20 \left(\log_{10} \frac{(V_2^2 + V_3^2 + V_4^2 + V_5^2)^{0.5}}{V_{in}} \right)$$
 - Inputs are full scale less 0.5dB. No channel advance.
 - A/D sample rate = 500kHz (416B,E,G), 5MHz (416D,K), 2MHz (416F), 10MHz (416H), 250kHz (416J), 190kHz (416L,M)
 - Crystal oscillator is used.
- The rates shown for sequential sampling are the maximum A/D converter start rates and include MUX sequencing and settling. For example, if four channels of the PCI-416E were scanned, the maximum sample rate on any one channel would be 2μs x 4 channels = 8μs (125kHz per channel).
- For fastest response on the analog comparator trigger, keep the reference voltage near the trip input voltage. To avoid overload recovery delays, do not let the trip input (or any other analog input) exceed ±10V.

- Allow 20 minutes warmup time to rated specifications for models PCI-416B,G,M,N.
- Use the crystal oscillator for best harmonic performance.
- Avoid mixing external triggers which are a close submultiple of the internal A/D start clock to prevent sample jitter.
- The BNC connector may be rewired to either external trigger or external A/D clock.
- PCI-416J and 416L bipolar input is user-selectable ±5V or ±10V (default) per channel. Total gain error over temperature range is ±4 LSB maximum. Total zero/offset error over temperature range is ±4 LSB maximum. Monotonicity: no missing codes over temperature range.
- Input polarity. Some models are fixed as bipolar only whereas others are user-selectable unipolar or bipolar. Still others require separate model numbers.
- PCI-416D, H, K, and M inputs are jumpered as single-ended. Special, user-configured wiring allows differential operation. Contact DATEL.
- Models F, G, J, K, L, M, and N use one A/D converter per channel.
- The customer must use shielded cables to insure EMC compliance.
- A/D-per-channel boards (models F, G, J, K, L, M, N) may be operated in "software differential" mode. Two A/D's are applied to the high and low legs of a single differential input channel. The two data values are then algebraically subtracted, either on the fly in real time or after all samples have been stored. Channel capacity in "software differential" is one-half the number of single-ended channels.

This technique offers excellent bandwidth, high common mode rejection and optional mix of single-ended and differential channels.

Marker Input

When selected in the Command Register, the marker input is for tagging A/D samples to an external event such as a clock timebase. The marker sets bit 15 of the A/D word to logic "1" for one sample clock cycle. Lower A/D bits still retain sign extension polarity. This tag is now stored in the FIFO along with the A/D sample. The user may do this as often as needed, and the marker can be asynchronous with the A/D sample clock. Post processing software then searches through the saved data to find each marked sample. The marker bit is not available for 16-bit A/D's.

| | | |
|----|----------|----------|
| 15 | 14 - 11 | 10 - 0 |
| M | Sign/MSB | A/D Data |

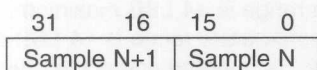
Marker input sets bit 15 = 1. Otherwise, bit 15 = 0.
(12-bit A/D shown)

Figure 2. Marker Sample Tagging

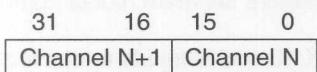
A/D Data Format

A/D data is delivered as a stream from the FIFO memory. For multichannel inputs, this means that data is multiplexed by the channel address with a modulo address wrap-around at the top channel. For example, with 4-channel inputs, the output channel sequence is 0, 1, 2, 3, 0, 1, . . . One additional factor is that the 32-bit wide dual FIFO contains two A/D samples. Therefore the longword sequence is 0,1 . . . 2,3 . . . 0,1 . . .

The FIFO output can take two formats depending on which analog module is used and whether single-channel or autosequential (autoincrement) channel addressing is selected. For single-channel mode, data appears as follows:



If the addressing is selected for autoincrement, data appears this way:



Note that all A/D data is right-justified within the 16-bit data word with sign extension to bit 15 or 31. Also be aware that the PCI-416 uses "Intel" or little-endian addressing where lower (or earlier) data is lower in word memory.

PCI-416SET/SRC SETUP/CONFIGURATION SOFTWARE

PCI-416SET/SRC is an MS-DOS example program and data recorder written mostly in "C". The program fully exercises and self-tests the board. It also serves as an excellent software library if you wish to make modifications. The executable PCI-416SET is included with PCI-416SRC.

- Performs PCI BIOS verification and setup
- Automatically configures to the display adapter, CPU and memory
- Initializes the interrupt and bus master systems and D/A output
- Allocates base or extended memory
- Performs self-test and A/D-D/A calibration
- Configures A/D sample rate, frame rate and sample counter
- Selects trigger mode and bus master or I/O block transfer
- Selects disk file output format to integer binary
- Saves data to base memory, extended memory or disk
- Full source code in "C" and assembly is available

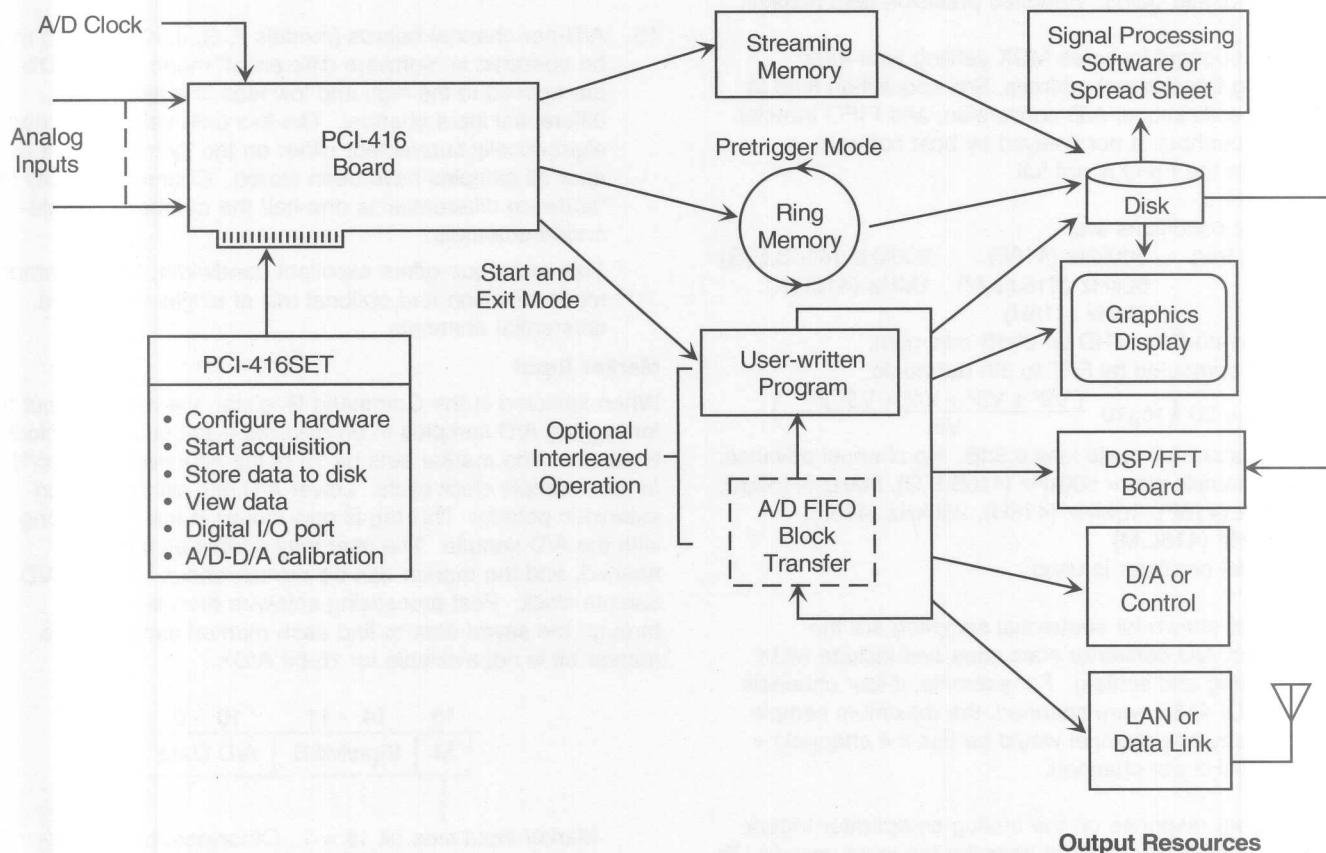


Figure 3. PCI-416SET Data Flow

Pre/Post Trigger Transient Capture Applications

A certain class of applications requires data sampled relative to one or more external events. Data before and after the event need to be analyzed. If the exact time of those external events cannot be predicted accurately but the event can be identified with a trigger, data must be recorded continuously then processed after the event occurred. At higher sample rates, the user must use all memory storage which has limited capacity but is still large enough to capture the event. A ring buffer circular storage method is used where new samples continually overwrite the oldest samples.

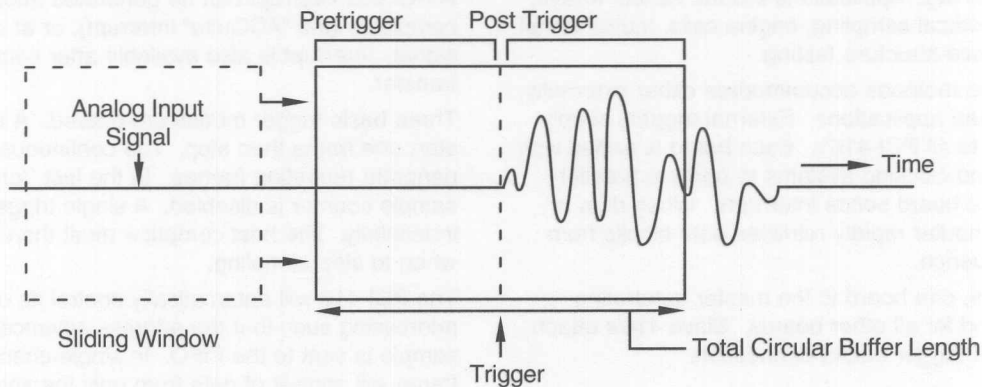


Figure 4. Transient Signal Capture

The PCI-416 accepts either a digital or analog (threshold trip) event trigger. An on-board D/A converter sets the comparator voltage level for the analog trigger. The system stores data before and after the trigger. A post trigger sample counter selects the number of offset samples after the trigger. The number of pretrigger samples equals the total circular storage minus the post trigger size. Note that pretrigger samples in Figure 5 are skewed over the buffer tail.

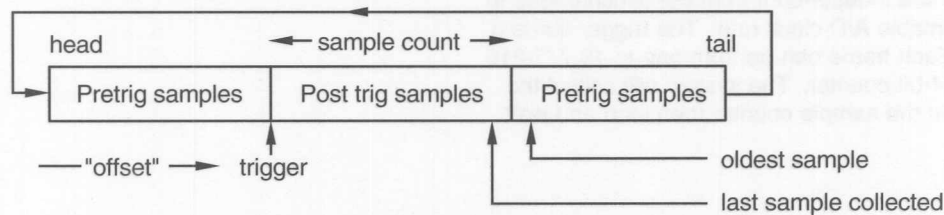


Figure 5. A/D Data Ring Buffering

A/D collection continues after the trigger until the system has stored the number of samples specified in the sample counter. The trigger sample can be found using backwards circular offset from the last sample saved. Multiple external events can be identified using a combination of the post trigger method and the marker inputs.

Special software available for the PCI-416 can access huge PCI memory. This requires the 80486 or Pentium CPU to enter protected mode and transfer the data. Collected A/D samples can then be saved to disk or tape.

System Throughput

All specifications listed here describe performance available on the *board*. Actual transfer rates out to system memory, disk, network, or other data destinations depend on many other factors. These include the memory type and memory controller, host software Operating System, disk interface, number of disk drives, buffer sizes, type of disk controller, number and method of simultaneous applications, DMA usage, CPU type and speed, bus loading, software design, etc. It is not practical to state a single set of performance specifications for the total *system* however, DATEL can give you guidelines for a specific configuration. For speed-critical applications, the full system must be thoroughly tested to develop actual performance.

Highly Parallel Array Sampling

Although the F, G, J, K, L, and N models of the PCI-416 offer unique high-performance simultaneous-sampling capabilities, this can be extended by connecting several PCI-416's in parallel. A master PCI-416 can distribute its internal trigger signal to several other 416's for concurrent sampling with practically no phase lag. Applications include sensor arrays, astrophysics, biomedical sampling, engine cells, multichannel audio, and aerospace structure testing.

Two interconnection methods accommodate either externally or internally triggered applications. External triggers simply connect in parallel to all PCI-416's. Each board is armed with its sample count and clocking systems to perform parallel sampling. Only one board sends interrupts. When data is ready, the host computer rapidly retrieves data blocks from each board in sequence.

For internal triggers, one board is the master generating triggers for itself and for all other boards. Slave 416's attach to the master 416's trigger output connection.

Trigger and Sample Count Systems

The PCI-416 accepts one of three triggers - external analog, internal or external digital. All three initiate identical internal actions. For the internally generated trigger, either a single trigger can be accepted ("single trigger mode") or the trigger can repeat ("continuous trigger mode") with programmable delays between each trigger.

Internal trigger rates are independent from but synchronous to the internal programmable A/D clock rate. The trigger starts a frame of samples. Each frame can be from one to 16,777,216 samples using the 24-bit counter. The system will collect the number of samples in the sample counter then stop and wait

for the next trigger. Meanwhile, the sample counter will automatically reload in anticipation of the next trigger. Data flows into the FIFO memory which will notify the host that it has data to be saved. The FIFO size is independent of the frame size, therefore FIFO flags will occur separately from the sample counter.

A PCI bus interrupt can be generated after each frame completes (the "ACquire" interrupt), or at each FIFO half full signal. Interrupt is also available after each bus master block transfer.

Three basic trigger modes are offered. A single trigger will start one frame then stop. The continuous trigger mode will generate repeating frames. In the last "forever" mode, the sample counter is disabled. A single trigger will start sampling indefinitely. The host computer must then externally decide when to stop sampling.

The PCI-416 will automatically control its own channel addressing such that the address advances immediately as a sample is sent to the FIFO. In single-channel mode, each frame will consist of data from only the selected channel. In automatic sequential addressing ("autoincrement"), the frame will contain one or more scans of channels, with addresses automatically wrapping around according to the channel capacity of the analog module.

The combination of programmable sample count, frame rate, A/D rate, and channel addressing mean that practically all conceivable applications can be done. The basic system timing is shown in Figure 8.

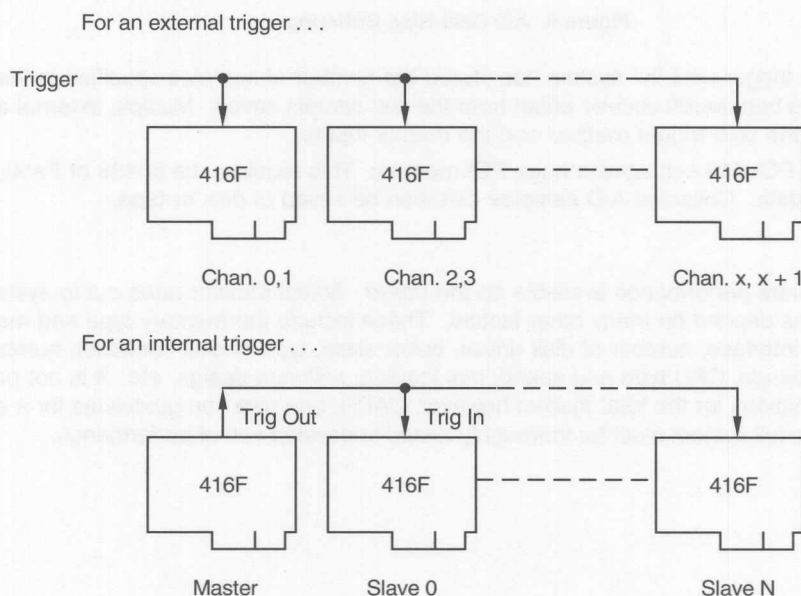


Figure 6. Highly Parallel Simultaneous Sampling

Start and Exit Mode

For applications which need the data streaming continuously to external software, the extensive library functions can easily be interleaved with user-written code. A special "start and exit" mode in PCI-416SET simply configures the board via menus, starts A/D conversion then exits to the operating system without saving any data. Next, the user's following program (usually in a batch file) retrieves data directly from the on-board registers or via 32-bit bus master mode. This is simple to program and very high speed. This data collection program may loop back repeatedly to get fast blocks of data and the PCI-416 continues filling the FIFO while the user program runs. This is true concurrent coprocessing with no lost data.

Start and exit mode offers a high degree of control over the board while avoiding time-consuming menu design and coding. The system will even wait for an external trigger, giving time to set up the data collection program. Start and exit mode can be saved to automatically run, like all other PCI-416SET applications. A typical program flow for start and exit is shown:

1. SETUP PCI-416 board.
2. Save configuration to disk.
3. Start A/D and exit to MS-DOS (the A/D stays running).
`<start of user's program>`
 LOOP:
- 4. If the FIFO overflowed, process the error.

5. Move block of A/D data from FIFO to host memory.
6. Do other processing on A/D data block (math, disk, display, etc.).
7. If more data is needed, GO TO LOOP.
8. Else, stop the A/D and quit.

The "Do other processing ..." step is a program written by the user. Notice that the PCI-416 continues with non-stop A/D sampling during this step.

Besides being a fast data recorder, PCI-416SET also performs register tests to verify proper board operation. In addition, PCI-416SET does calibration using an external dc voltage source, loads data into the D/A channel and exercises the digital I/O port.

The source code may be modified by the user (or by DATEL under special order) to adapt to any conceivable function.

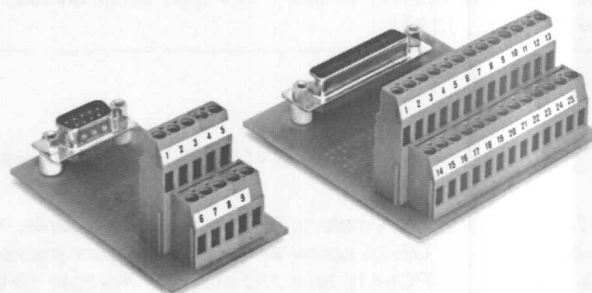


Figure 7. PC-490A and PC-490B D-Connector to Screw Terminal Adapters

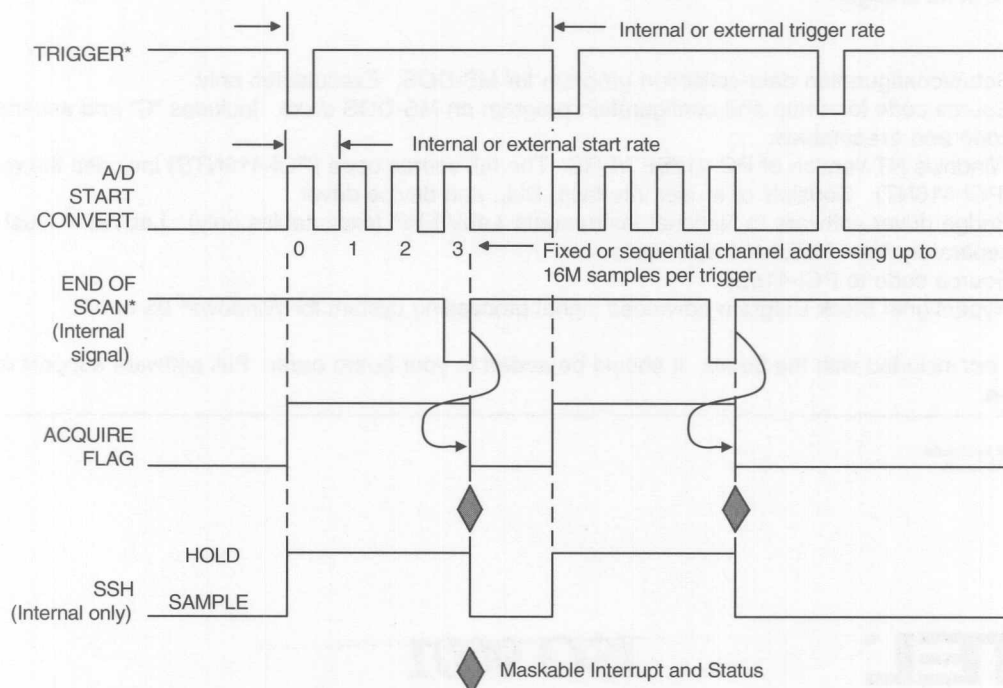
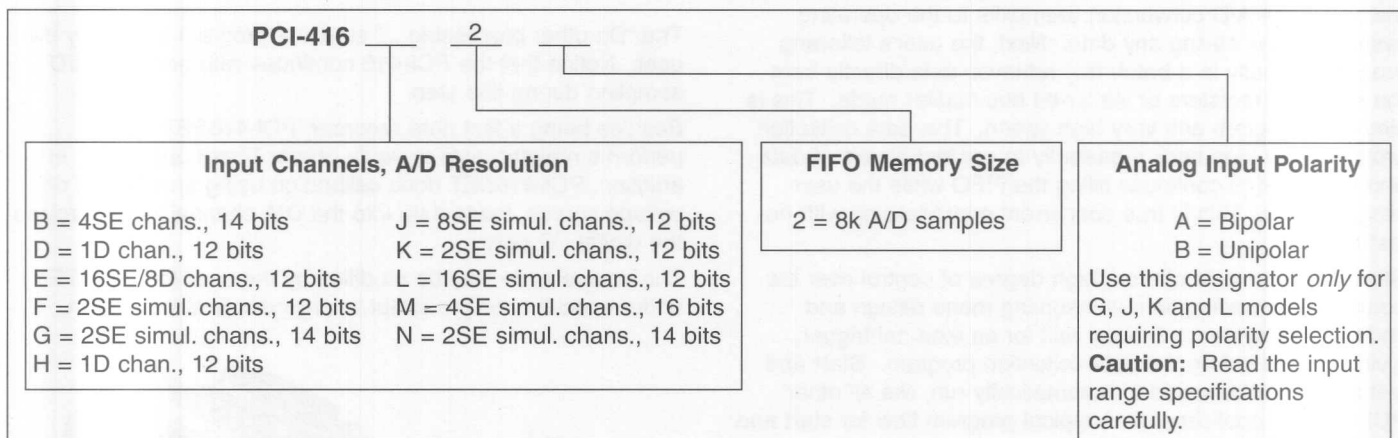


Figure 8. PCI-416 Timing Diagram

ORDERING INFORMATION



Example: PCI-416G2A 2 simul. channels, 14-bit 1MHz A/D's, 8k FIFO, ±5V input

| | |
|------------|--|
| 61-7342340 | SMA male to BNC male coaxial cable, 1 meter length. One cable required per channel. |
| PC-490B | DB-25 screw termination adapter (cable not included). Not recommended for high frequency signals. |
| PCI-30259 | PCI-416 less A/D module. Accepts 16-bit high-speed digital input and strobe at the module sockets. |
| PCI-30264 | PCI-416J2 with 380kHz sampling per channel. |
| PCI-30267 | PCI-416G2 with 2MHz sampling per channel. |
| UM-PCI-416 | Spare user manual. One is included with board. |

Each board is power-cycle burned-in, tested and calibrated. All models include a user's manual. An example program disk is available on request at no charge.

Software:

| | |
|----------------|--|
| PCI-416SET | Setup/configuration data-collection program for MS-DOS. Executables only. |
| PCI-416SRC | Source code for setup and configuration program on MS-DOS disks. Includes "C" and assembly source code and executables. |
| PCI-416NT, NTS | Windows NT version of PC-416SET/SRC. The full source code (PCI-416NTS) includes the executables (PCI-416NT). Consists of a user interface, DLL, and device driver. |
| PCI-416LV | Bridge driver software to National Instruments' LabVIEW® (executables only). LabVIEW must be purchased separately from National Instruments |
| PCI-416LVS | Source code to PCI-416LV. |
| Call DATEL | Hypersignal Block Diagram advanced signal processing system for Windows® 95 or NT. |

Note: Software is *not* included with the board. It should be added to your board order. Full software support is available only with board purchase.

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Windows and MS-DOS are Microsoft trademarks
LabVIEW is a National Instruments trademark

